Comparison of Phase-Shifted and Level-Shifted PWM in the Modular Multilevel Converter

Rosheila Darus[1,2], Georgios Konstantinou[1], Josep Pou[1,3], Salvador Ceballos[4] and Vassilios G. Agelidis[1]
[1] Australian Energy Research Institute (AERI) & School of Electrical Engineering and Telecommunications
The University of New South Wales, Sydney, NSW, 2052, Australia.
[2] Faculty of Electrical Engineering, Universiti Teknologi Mara (UiTM), 40450 Shah Alam, Selangor, Malaysia.
[3]Terrassa Industrial Electronics Group (TIEG), Technical University of Catalonia, Catalonia, Spain.
[4]TECNALIA, Energy Unit, Basque Country, Spain.
email: r.darus@student.unsw.edu.au g.konstantinou@unsw.edu.au j.pou@unsw.edu.au salvador.ceballos@tecnalia.com
vassilios.agelidis@unsw.edu.au

***Abstract*—This paper reports a comparison study of different carrier-based PWM techniques applied to the modular multilevel converter. Phase-disposition PWM (PD-PWM) and phase-shifted pulse-width modulation (PS-PWM) with non-interleaving and interleaving are considered in this study. In PS-PWM, two cases are evaluated. In the first case, the particular SMs that have to be activated/deactivated are defined by a voltage balancing algorithm, which is the same one implemented in PD-PWM. In addition, an algorithm to restrict the number of switching SMs is also implemented to reduce the switching frequency of the power devices. In the other case of PS-PWM, each sub-module (SM) has a carrier signal associated to it and capacitor voltage balance is achieved by individual control of its capacitor voltage. The circulating current is controlled to be a dc component in all the cases. Simulation and experimental results are presented to evaluate the quality of the line-to-line output voltages and SM capacitor voltage ripples for the different cases under study.**

***Index Terms*—Modular multilevel converter, Modulation technique, Circulating current control, Capacitor voltage balancing**

I. INTRODUCTION

The modular multilevel converter (MMC) is the preferred topology for high voltage (HV) applications because of its modularity and higher voltage ratings. Other advantages of the MMC are the quality of the output voltages, that capacitor voltage balance can be easily implemented, the fault tolerant operation capability, and the elimination of the dc-link capacitor [1]–[4].

The MMC (Fig. 1) consists of a series of N sub-modules (SMs), usually based on the half-bridge circuit, each of them including a capacitor as a voltage source. Configurations with energy storage are also possible [5]. A circulating current exists within each phase-leg of the MMC and has a significant impact on the ratings of the power devices, capacitors voltage ripples and power losses [6]. A circulating current control is necessary to reduce such an impact.

A wide range of modulation techniques can be applied to the MMC, mainly depending on the number of SMs in the phase-legs of the converter. The most common ones are carrier-based PWM (CB-PWM) [7] either phase-shifted PWM (PS-PWM) [8]–[11] or level-shifted PWM (LS-PWM) [11]–[13]. Other techniques include SHE-PWM [14] and band-tolerance modulation based on hysteresis [15]. As a result of its better harmonic performance, phase-disposition PWM (PD-PWM) is the preferred choice of LS-PWM technique in MMCs.

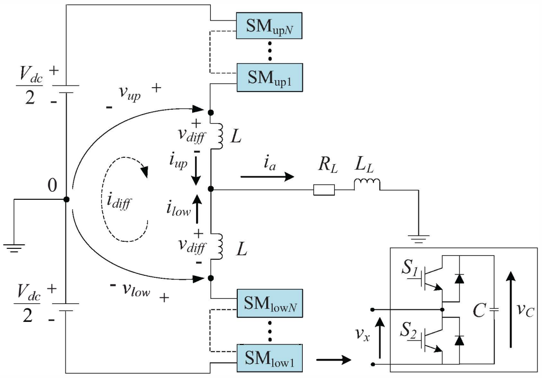

Fig. 1. Phase-leg MMC.

An interesting property of the MMC, owing to its two-arm configuration, is that it can generate two different number of voltage levels for the same number of SMs per arm [11]. The most straightforward way of deriving the additional number of levels is through interleaving of the carriers [10] between the upper and lower arms while maintaining the effective switching frequency of each SM constant.

Capacitor voltage balancing is also required to keep the capacitors voltages at the reference value. A common way to perform capacitor voltage balance is based on sorting the capacitor voltage values from the highest to the lowest or vice versa, and making a decision on the SMs to be activated/deactivated considering the direction of the arm current [16]. A separate voltage balancing algorithm might not be necessary if the modulation technique can provide approximately equal conduction periods [13] per SM (i.e. PS-PWM). Voltage balancing can also be achieved through capacitor voltage estimation and energy averaging.

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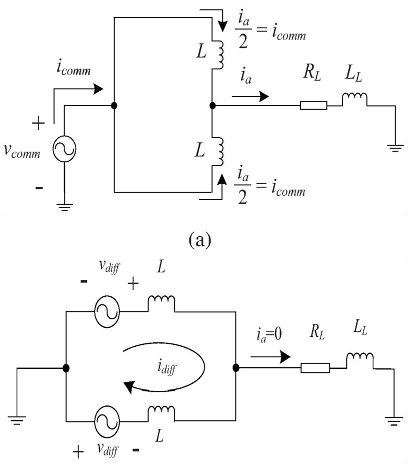

(a)

(b)

Fig. 2. (a) Common mode and (b) Differential mode circuits.

Although CB-PWM techniques have been extensively analysed in the literature, a complete comparison and evaluation when considering carrier interleaving and the voltage balancing algorithms has not been presented. The purpose of this paper is to compare CB-PWM techniques, including the application of carrier interleaving and demonstrate the benefits of the sorting stage in the voltage balancing of the MMC.

The paper is structured as follows. The MMC circuit analysis, circulating current control and modulation techniques used in this study are introduced in Section II. The two capacitor voltage balancing algorithms are presented in Section III, followed by simulation and experimental results and comparison in Section IV. The conclusions of the work are summarised in Section V.

II. MMC, CIRCULATING CURRENT CONTROL AND MODULATION TECHNIQUES

Two independent circuits can be obtained from the analysis of a phase-leg of the MMC (Fig. 1), the common mode and differential mode, as shown in Figs. 2(a) and (b) respectively. The two circuits can be analyzed separately and do not affect each other [17]. The common and differential voltages (v_{comm} and v_{diff}) and currents (i_{comm} and i_{diff}) are:

$$v_{comm} = \frac{v_{up} + v_{low}}{2}, \qquad v_{diff} = \frac{v_{up} - v_{low}}{2} \tag{1}$$

$$i_{comm} = \frac{i_{up} + i_{low}}{2}, \qquad i_{diff} = \frac{i_{up} - i_{low}}{2}. \tag{2}$$

The differential (or circulating) current i_{diff} circulates within the arms of the MMC and does not appear in the output. It consists of a dc and ac components [17]. The dc component is essential to keep the phase-leg energised but the ac components can be eliminated, reducing the losses and increasing the efficiency of the MMC.

The circulating current can be controlled by imposing a differential voltage (v_{diff}). Fig. 3 shows a control loop where the power provided by the phase-leg is calculated and used to estimate the circulating current reference. A moving average filter (MAF) extracts the dc component of the instantaneous power. The average voltage in the SM capacitors of the phase-leg provides additional information to the circulating current reference and is used to regulate the capacitor voltages at the reference value. The final circulating current reference is provided to a control loop based on proportional controller (k_p).

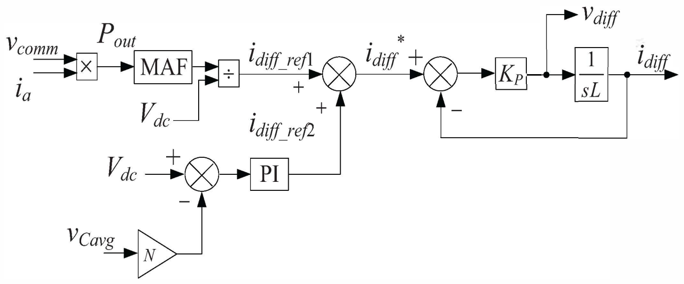

Fig. 3. Circulating current control.

The next step in the control of a phase-leg includes the PWM technique. Its main task is to define the total number of SMs that are activated in the upper and lower arms. Three different carrier dispositions for LS-PWM are usually considered in the literature: (i) PD-PWM, (ii) phase-opposition-disposition PWM (POD-PWM), and (iii) alternating phase-opposition-disposition PWM (APOD) [11]. N additional output voltage levels can be achieved through interleaving the carriers of the upper and lower arm within the same phase-leg. In most cases, the gating signals are not directly derived from the modulation technique as a capacitor voltage balancing stage is usually required.

III. VOLTAGE BALANCING ALGORITHM

Selection of the SMs depends on the SM capacitor voltages and the direction of the arm currents so that the voltages are regulated towards the reference. When the number of activated SMs within an arm increases, the SMs with lowest/highest voltages will be activated if the current direction is such that it charges/discharges the capacitors. However, such an approach may lead to unnecessary switching operations [16] and therefore increased switching losses in the power devices if no additional restriction is taken. This can be avoided if the sorting stage uses virtual voltage values that also depend on whether SM is activated or not [20] effectively reducing the unnecessary transitions and limiting the switching frequency of each SM (Fig. 4). The modified voltages seen by the voltage sorting are expressed with:

$$v'_{Cupj} = -sgn(i_{up}) \times v_{Cupj}, \tag{3}$$

$$v''_{Cupj} = v'_{Cupj} + s_{upj}\Delta K, \tag{4}$$

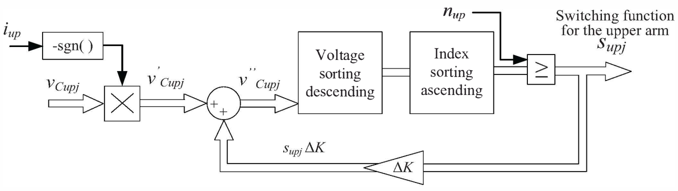

Fig. 4. Restricted voltage balancing algorithm for the upper arm.

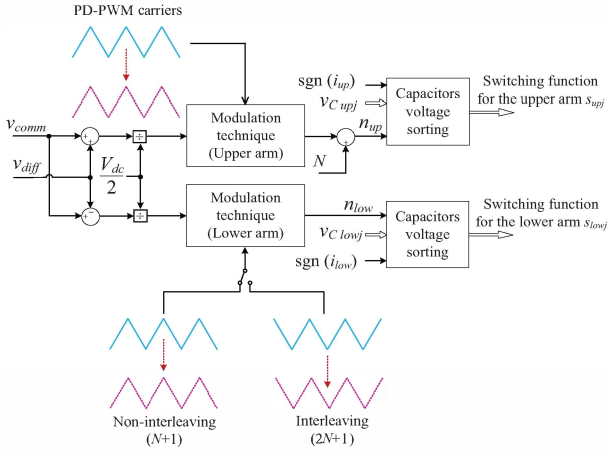
PD-PWM carriers
v_{comm}
v_{diff}
V_{dc}
2
÷
Modulation technique (Upper arm)
Modulation technique (Lower arm)
sgn (i_{up})
$v_{C\,upj}$
n_{up}
N
Capacitors voltage sorting
Switching function for the upper arm s_{upj}
n_{low}
$v_{C\,lowj}$
sgn (i_{low})
Switching function for the lower arm s_{lowj}
Non-interleaving (N+1)
Interleaving (2N+1)

Fig. 5. PD-PWM with non-interleaving and interleaving between the arms with voltage sorting algorithm with N carriers.

A. PD-PWM with Restricted Voltage Balancing Algorithm

The main principles of PD-PWM have been explained in detailed in [7]. In the MMC, the number of carriers is equal to the number of SMs per arm (N) and all the carrier waveforms are in phase [11]. Interleaving of the upper and lower arm can be achieved by phase-shifting the carriers of the upper and lower arm by 180 degrees. The implementation of the current control, PD-PWM stage and capacitor voltage balancing algorithm is shown in Fig. 5.

B. PS-PWM with Restricted Voltage Balancing Algorithm

PS-PWM also requires N carrier waveforms per arm. Unlike LS-PWM, the carriers cover the whole range of modulation indices with consecutive carriers phase-shifted by $2\pi/N$, as shown in Fig. 6. The number of SMs to be activated in the arm is determined by the number of carrier signals that are below the reference signal at any given time. Interleaving is achieved by phase-shifting $2N$ carriers by π/N and distributing them alternatively between the upper and the lower arm, again with N carriers defining the transitions of each arm. The carrier frequency for PS-PWM is selected based on:

$$f_{c(PS-PWM)} = \frac{f_{fc(PD-PWM)}}{N} \tag{5}$$

so that the average switching frequency of each SM is equal to that of the PD-PWM technique of Subsection III-A.

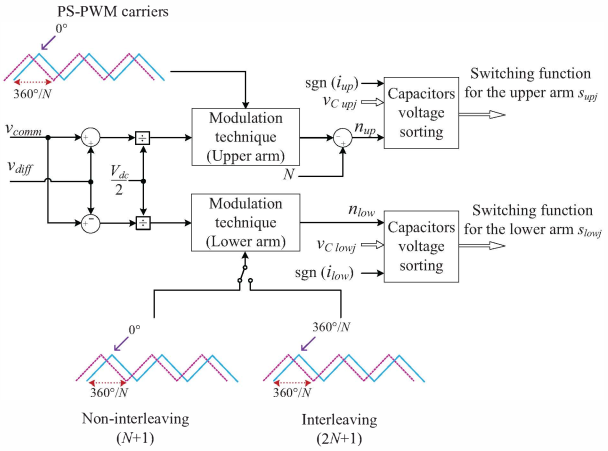

Fig. 6. PS-PWM for non-interleaving and interleaving between the arms with voltage sorting algorithm with N carriers.

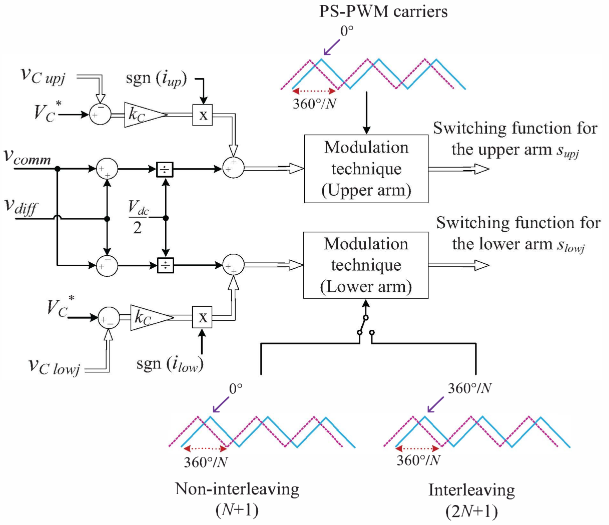

Fig. 7. PS-PWM for non-interleaving and interleaving between the arms with individual capacitor voltage control with N carriers.

C. PS-PWM with Individual Capacitor Voltage Control

Alternatively to the sorting stage, voltage balancing can be achieved with PS-PWM where each carrier waveform is directly associated with one particular SM [13]. Additional compensation and feedback loops are also required to modify the individual PWM reference signal driving the capacitor voltages towards the reference value. The implemenation of PS-PWM without the sorting algorithm is shown in Fig. 7. Interleaving between the upper and lower arms is similar to that in Subsection III-B. This approach is only valid with PS-PWM as LS-PWM patterns do not provide the required equal conduction times and capacitor voltage balancing cannot be achieved [11].

TABLE I
MMC SIMULATION PARAMETERS

Parameter	Value
Number of SMs per arm, N	10
Dc-link voltage, V_{dc}	6000 V
SM reference voltage, V_C	600 V
SM capacitor, C	1.5 mH
Arm inductors, L	18 mH
Carrier frequency PD-PWM, f_c	3 kHz
Carrier frequency PS-PWM, f_c	300 Hz

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

The analysis and comparison of the PWM techniques is based on an MMC with ten SMs per arm (N=10) using the parameters of Table I. An average switching frequency of 300 Hz per SM is selected as a balance between producing low switching power losses and the upper SM switching frequency ratio limit of approximately 10, above which no observable gain in harmonic and capacitor voltage ripple is observed [9]. A constant *RL* load is considered at the output of the MMC.

The capacitor voltages of the upper arm (v_{Cupj}) for all three PWM techniques, both without and with carrier interleaving, are shown in Fig. 8(a)-(f) for an operating point of m_a=0.95. The use of carrier interleaving has a negligible effect in the capacitor voltage ripple which is mainly driven by the average switching frequency of the SMs and the operating point of the converter [21], [22]. As the average SM switching frequency is approximately equal for all techniques, the peak-to-peak SM capacitor voltage ripple ($v_{Cupj_{pp}}$) is also similar at any operating point (Fig. 9).

Despite the fact that all techniques yield the same $v_{Cupj_{pp}}$, the lack of a sorting algorithm results in higher deviations among the SM capacitor voltages of the same arm as seen in Figs. 8 (e) and (f). This is also demonstrated in Fig. 10 where the absolute capacitor voltage deviation from the reference for the PS-PWM with individual capacitor voltage control lies well above the two PWM techniques based on the sorting algorithm.

Interleaving of carriers results in a continuous variation of the number of SMs that is connected to the phase-leg between $N-1$, N and $N+1$ [12]. A direct effect of this variation is observed in the arm currents of PWM techniques with interleaving, resulting in higher harmonic content and, hence, higher RMS value the arm current, slightly increasing the overall losses. The currents of the upper and lower arm under non-interleaving and interleaving PWM techniques are given in Fig. 11

The line-to-line voltages for all six cases for an operating point of m_a=0.95 are presented in Fig. 12. The higher number of output voltage levels for MMCs with carrier interleaving can be observed. Other characteristics of the PWM techniques at this operating point, including the average SM switching frequency and peak-to-peak capacitor voltage ripple are summarised in Table II. The harmonic spectra of the line-to-line voltages are given in Fig. 13.

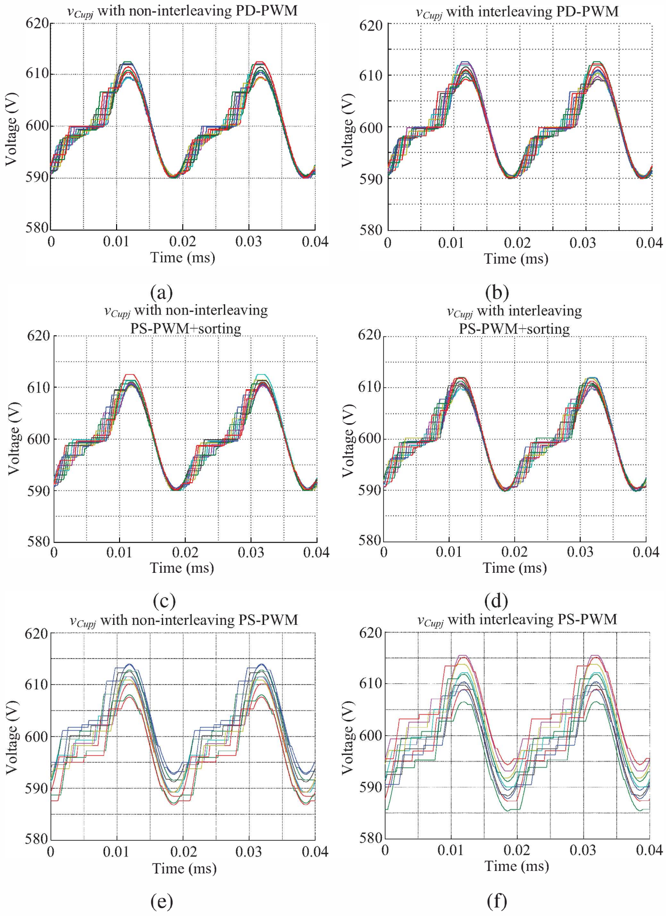

Fig. 8. Capacitors voltages (v_{C_upj}): (a) with non-interleaving PD-PWM, (b) with interleaving PD-PWM, (c) with non-interleaving PS-PWM+sorting, (d) with interleaving PS-PWM+sorting, (e) with non-interleaving PS-PWM and (f) with interleaving PS-PWM.

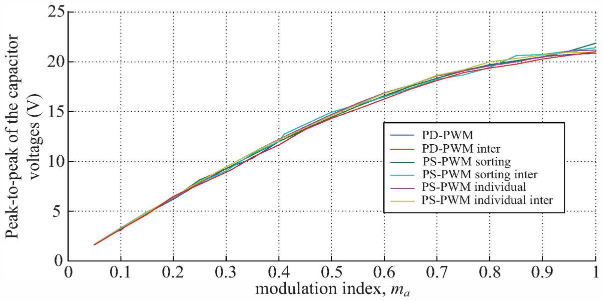

Fig. 9. Peak-to-peak capacitor voltage ripple ($v_{Cupj_{pp}}$) vs modulation index with a constant RL load.

The higher number of levels, as a result of carrier interleaving, provides an improved overall performance compared to the non-interleaved PWM techniques albeit with increased arm current harmonics and RMS value. The interleaved techniques exhibit similar %THD for the common mode voltage (Fig. 14) where there is a gap of THD values between non-interleaving

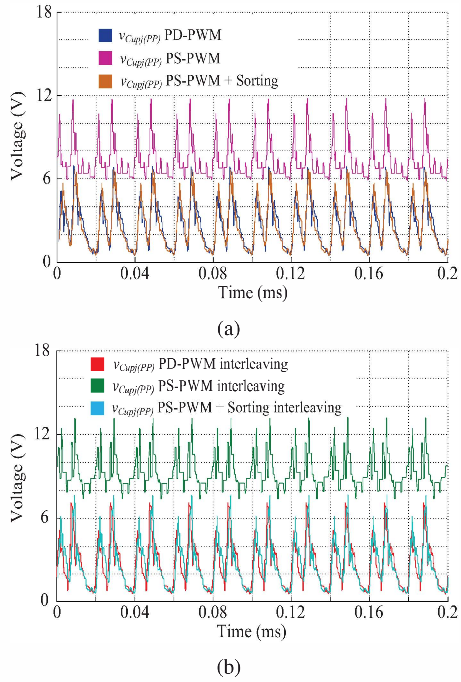

Fig. 10. Deviation size of the capacitor voltages in the upper arm ($v_{Cupj_{PP}}$): (a) with carrier non-interleaving and (b) with carrier interleaving.

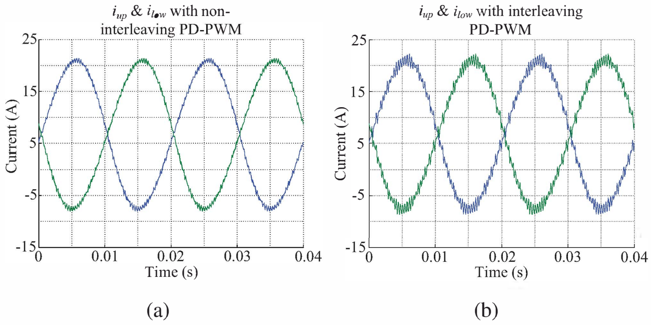

Fig. 11. Upper and lower arm currents (i_{up} & i_{low}): (a) with non-interleaving PD-PWM and (b) with interleaving PD-PWM.

and interleaving, with interleaved producing lower THD. On the other hand, when interleaving between the arms of the converter is not applied, PD-PWM demonstrates a better line-to-line common voltage compared to PS-PWM techniques in terms of %THD and %WTHD as a result of the harmonic cancellation in the line-to line voltages (Fig. 14 and Fig. 15).

B. Experimental Verification

Experimental results are obtained from a laboratory prototype of an MMC phase-leg with five SMs per-arm. Interleaving produces eleven levels ($2N$-1) at the output voltages, while non-interleaving produces six levels only (N-1), as shown in Fig. 16. Interleaving also affects the output current by reducing the current ripple. On the other hand, interleaving increases the ripple in the arm currents and the circulating current (Fig. 17).

PD-PWM with restricted voltage balancing has better control to keep the SM capacitor voltages at the reference value. The peak-to-peak capacitor voltage value is similar either using PD-PWM with restricted voltage balancing or PS-PWM with individual capacitor voltage as shown in Fig. 18. Notice though that the SM capacitor voltages operating with PS-PWM in Fig. 18(b) are more disperse than those in Fig. 18(a) with PD-PWM.

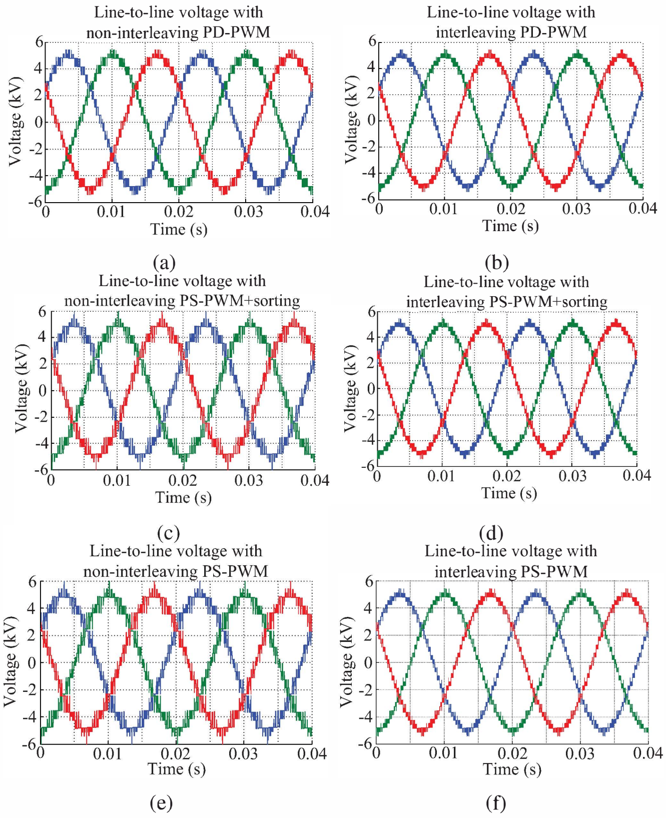

Fig. 12. Line-to-line voltage (v_{LL}): (a) with non-interleaving PD-PWM, (b) with interleaving PD-PWM, (c) with non-interleaving PS-PWM+sorting, (d) with interleaving PS-PWM+sorting, (e) with non-interleaving PS-PWM and (f) with interleaving PS-PWM.

TABLE II
SIMULATION RESULTS WITH NON-INTERLEAVING AND INTERLEAVING TECHNIQUE

Modulation technique	$f_c(Hz)$	%THD $v_{LL_{comm}}$	$f_{sw}(Hz)$	Δv_{Cup} (V)
PD-PWM (Non-Inter.)	3000	5.98	345	20.70
PS-PWM (Non-Inter.)	300	8.77	343	21.37
PS-PWM+S (Non-Inter.)	300	8.76	340	20.68
PD-PWM (Interleaving)	3000	4.33	345	20.60
PS-PWM (Interleaving)	300	4.38	350	21.31
PS-PWM+S (Interleaving)	300	4.37	350	20.69

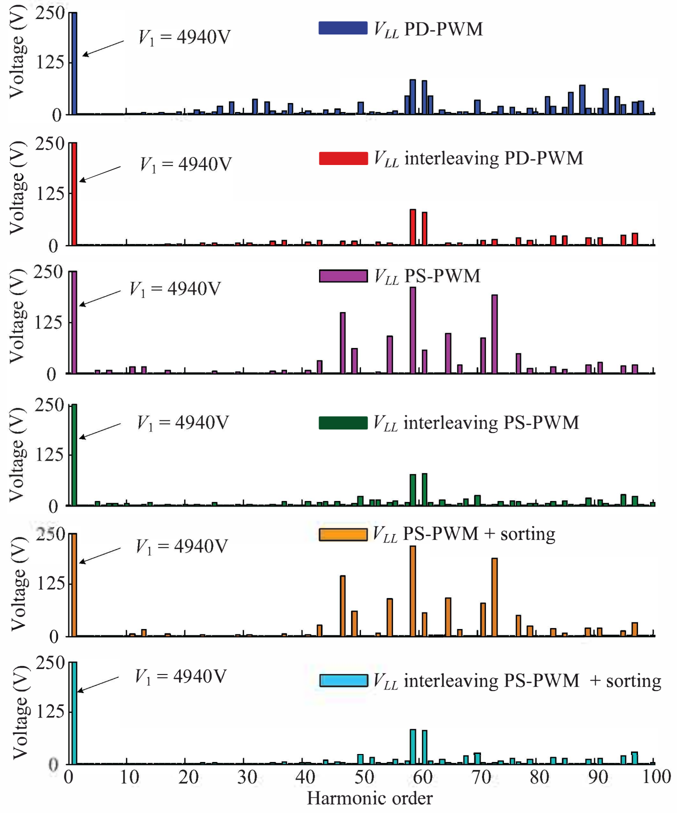

Fig. 13. Harmonic spectra of line-to-line common voltage ($V_{LL_{comm}}$) for all six cases.

V. CONCLUSION

n this paper, PD-PWM and PS-PWM have been applied to the MMC and evaluated considering non-interleaving and interleaving. Capacitor voltage balance under PS-PWM has been implemented using individual voltage control and a sorting algorithm like in PD-PWM. It has been shown that the sorting algorithm performs better in regulating the capacitor voltages in both cases PD-PWM and PS-PWM. Although the carriers' frequencies have been selected to produce similar switching frequencies to the power devices, PD-PWM produces better line-to-line output voltage spectra. The application of interleaving between the upper and the lower arms increases the quality of the output voltages and currents but produces more ripples in the arm currents and circulating current. This may force to increase the value of the arm inductors.

VI. ACKNOWLEDGEMENT

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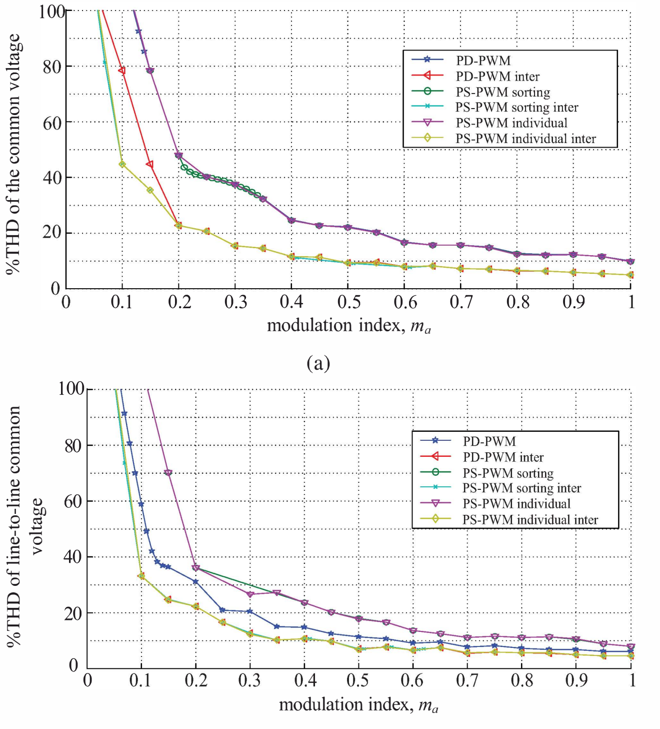
REFERENCES



(a)

(b)

Fig. 14. Total harmonic distortion: (a) common voltage and (b) line-to-line common voltage.

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bolognia Power Tech. Conf., Jun. 2003.*

[2] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended dc-bus-applications," in *Proc. IEEE IPEC*, 2010, pp. 502-507.

[3] R. Marquardt, "Modular multilevel converter topologies with DC-short circuit current limitation," in *Proc. IEEE ICPE* 2011, pp. 1425-1431.

[4] W. Jun, R. Burgos, and D. Boroyevich, "A survey on the modular multilevel converters - modeling, modulation and controls," in *Proc. IEEE ECCE*,2013, pp. 3984-3991.

[5] M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage" *IEEE Trans. Power Electron.*, early access, 2014, doi: 10.1109/TPEL.2014.2303297.

[6] J. W. Moon, C. S. Kim, J. W. Park, D. W. Kang, and J. M. Kim, "Circulating currrent control in MMC under the unbalanced voltage," *IEEE Trans. Power Del.*, vol. 28, pp. 1952-1959, Oct. 2013.

[7] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters; principles and practice*, IEEE press series on power engineering, 2003.

[8] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An improved control systemfor modular multilevel converters with new modulation strategy and voltage balancing control," *IEEE Trans. Power Electron.*, vol. doi: 10.1109/TPEL.2014.2304969, 2014.

[9] A. Hassanpoor, S. Norrga, H. Nee, and L. Angquist, "Evaluation of different carrier-based PWM methods for modular multilevel converters for HVDC application," in *Proc. IEEE IECON*, 2012, pp. 388-393.

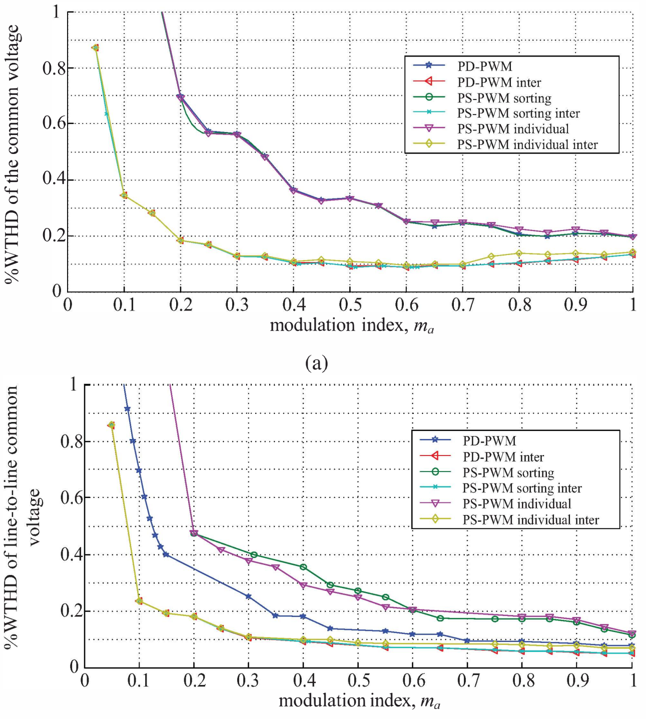
[10] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, and V. G. Agelidis, "Circulating current control and evaluation of carrier dispositions in modular multilevel converters," in *Proc. IEEE ECCE Asia*, Jun. 2013, pp. 332-338.

[11] G. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques," in *Proc. IEEE ICIEA*, 2009, pp. 3399-3404.

[12] G. Konstantinou, M. Ciobotaru, and V. G. Agelidis, "Analysis of multi-carrier PWM methods for back-to-back HVDC systems based on modular multilevel converters," in *Proc. IEEE IECON*, 2011, pp. 4391-4396.

[13] M. Hagiwara, and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, pp. 1737-1746, Jul. 2009.

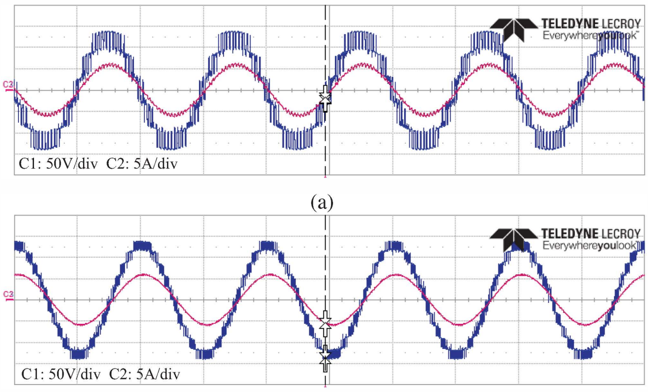
[14] G. Konstantinou, M. Ciobotaru, V. G. Agelidis, "Selective harmonic elimination pulse width modulation of the modular multilevel converter," *IET Power Electronics*, Vol. 6, No. 1, pp. , Jan. 2013.



(a)

(b)

Fig. 15. Percentage of weighted total harmonic distortion (%WTHD): (a) common voltage and (b) line-to-line common voltage.



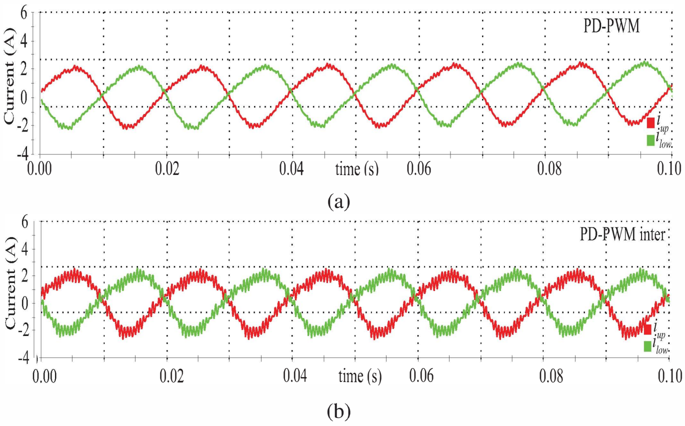
(a)

(b)

Fig. 16. Ouput voltage and current with constant RL load: (a) six levels output voltage using non-interleaving PD-PWM and (b) eleven levels output voltage using interleaving PD-PWM.

[15] A. Hassanpoor, L. Angquist, S. Norrga, K. Ilves, H.P. Nee, "Tolerance Band Modulation Methods for Modular Multilevel Converters "*IEEE Trans. Power Electron*, Early Access, 2014,

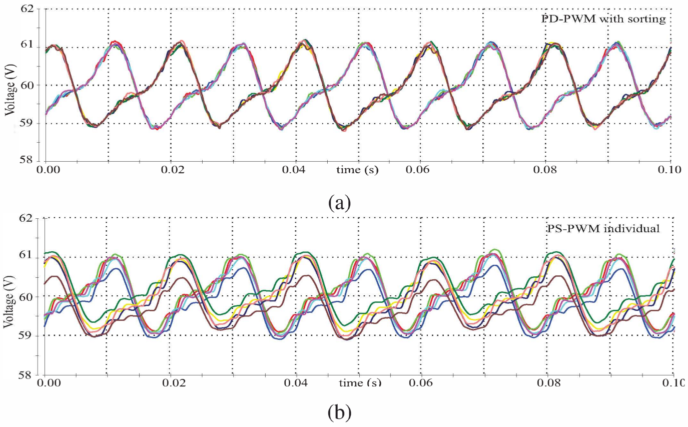
[16] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, pp. 2903-2912, Oct. 2010.



(a)

(b)

Fig. 17. Arm currents: (a) with non-interleaving PD-PWM and (b) with interleaving PD-PWM.



(a)

(b)

Fig. 18. Capacitors voltages: (a) using PD-PWM with restricted voltage balancing and (b) using PS-PWM with individual capacitor voltage control.

[17] J. Pou, S. Ceballos, J. Zaragoza, G. Konstantinou, and V. G. Agelidis, "Optimal injection of harmonics in circulating currents of modular multilevel converters," in *Proc. IEEE ISIE*, May 2013, pp. 1-7.

[18] S. Xu and A. Huang, "Circulating current control of double-star chopper-cell modular multilevel converter for HVDC system," in *Proc. IEEE IECON* 2012, pp. 1234-1239.

[19] A. Antonopoulos, L. Angquist, L. Harnefors, K. Ilves, and H. P. Nee, "Stability analysis of modular multilevel converters with open-loop control," *Proc. IEEE IECON*, Nov. 2013, pp. 6316-6321.

[20] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, and V. G. Agelidis, "A modified voltage balancing sorting algorithm for the modular multilevel converter; evaluation for staircase and phase-dispositon PD-PWM," in *Proc. IEEE APEC*, Mar. 2014.

[21] M. Vasiladiotis, N. Cherix and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters", *IEEE Trans. Power Electron.,* early access, doi: 10.1109/TPEL.2013.2286293, 2013.

[22] S. Ceballos, J. Pou, S. Choi, M. Saeedifard, and V. Agelidis, "Analysis of voltage balancing limits in modular multilevel converters," in *Proc. IEEE Industrial Electronics Conference (IECON'11)*, 7-10 Nov. 2011, Melbourne, Australia, pp. 4397-4402.